A 12-bit 5MS/s Synchronous SAR ADC With Error Correction

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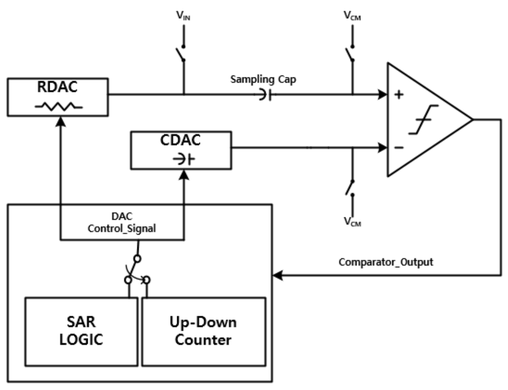
Introduction

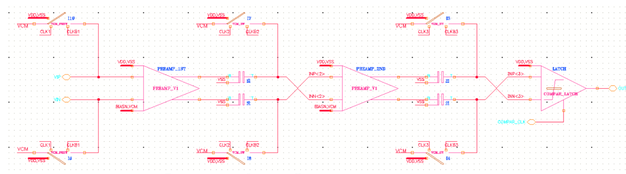
The SAR ADC (Successive Approximation Register Analog-to-Digital Converter) structure is widely used due to its advantages in high-resolution implementation and low power consumption. Additionally, its compact structure makes it conducive to increasing the operating speed by incorporating some useful techniques. However, designing low-power SAR ADCs can be challenging. A High-Performance Successive Approximation Register Analog-to- Digital Converter (SAR ADC) is presented in this work. The SAR ADC has trade-off between size and resolution specification. The array of passive devices in high resolution SAR ADC has a size problem because total capacitance or resistance of DAC increase exponentially with the ADC resolution. To overcome this issue, the proposed SAR ADC is used both capacitor array and resistor array. Because passive device matching is important to achieve a high performance SAR ADC, the proposed SAR ADC uses certain layout technique to attenuate mismatch of resistors. In addition, two digital logics are used in the to solve the settling time issue caused by using resistors.

Architecture



<Block Diagram of proposed SAR ADC>

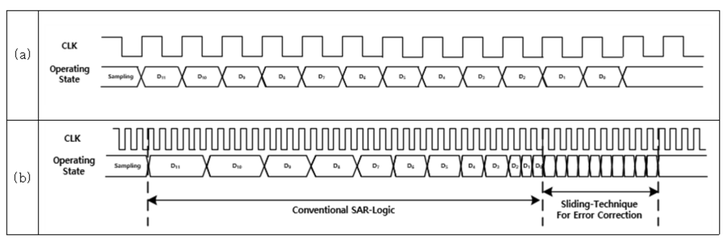
- The proposed SAR ADC is a single-structure synchronous ADC consisting of an RDAC, CDAC, Sample-and-Hold Circuit, Comparator, and Digital Logic Block.
- The R-C Hybrid DAC is a highly useful DAC structure for saving area, allowing for approximately 98% area reduction compared to using CDAC alone. Additionally, the RDAC offers the advantage of being shareable within the same SoC. To reduce errors caused by RDAC mismatch, the RDAC Layout utilizes the Cross-connected Layout technique.
- The S/H circuit samples the input signal during the sampling phase and maintains the sampled signal during the conversion phase. In the sampling phase, the top plate of the sampling capacitor is connected to the top plate of the CDAC with a VCM (500mV) reference voltage.
- The Comparator employs two pre-amplifiers to amplify the input signal and reduce input-referred noise, thereby increasing decision accuracy.



<schematic of comparator>

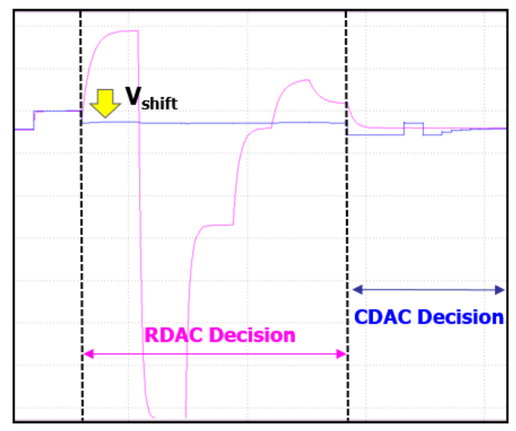
Method

- Uniform vs Non-uniform Decision Timing



  - (a) is uniform-decision timing.
  - (b) shows the conventional SAR Logic operation with Non-Uniform Decision Timing and error correction through Sliding-Technique during 10-cycle.

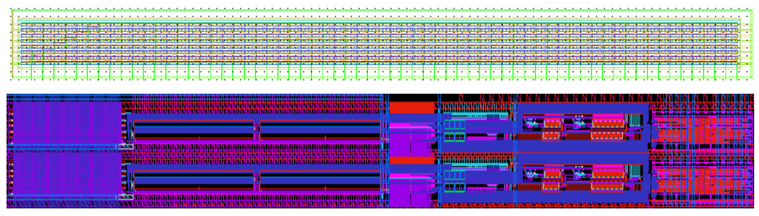
- ADEC



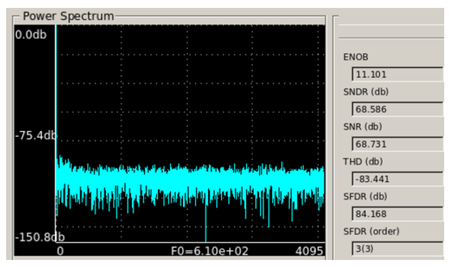
  - The above simulation results demonstrate the operation of the SAR ADC with the applied ADEC (Adaptive Decision-Error Correction) technique. ADEC is applied during the transition from coarse conversion to fine conversion.
  - ADEC improves the performance of the SAR ADC by addressing errors that may arise due to settling issues in previous bit decisions and allowing for their correction.

Result & Analysis

- Layout of Multi channel SAR-ADC & Resistor-DAC



- Simulation Result



  - In the case of ENOB, this is the result reflecting the linearity problem of the Vncap device of the LPP process.

Conclusions

- R-C Hybrid DAC that enables low-area and low-power design was used, and calibration was performed using non-uniform decision timing and LSB sliding technique to overcome the disadvantages caused by Resistor DAC
- A high resolution ADC was designed with a specification of 12bit 5Ms/s, and the target ENOB of 11bits or more was obtained.

References

[1] Chun-Cheng Liu, Soon-Jyh Chang, Guan-Ying Huang, Ying-Zu Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," IEEE J. of Solid State Circuits, Vol. 45, No.4, April 2010.

[2] Sang-Hyun Cho, Chang-Kyo Lee, Jong-Kee Kwon, and Seung-Tak Ryu "A 550-µW 10-b 40-MS/s SAR ADC With Multistep Addition-Only Digital Error Correction", IEEE J. of Solid State Circuits, Vol. 46, No.8, Aug. 2011, pp. 1881-1892

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